Remarks

Applicants thank the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title conforms to the claimed matter.

The amended specification includes reference to related patents and publications, and provides antecedent support for the term “register” used in the claims.

The new claims obviate the rejections under 35 USC 103. The new claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

New claim 32 defines a system.

A memory contains instructions.

A main processor unit is coupled to the memory and executes instructions obtained from the memory.

A stack machine is separate from the main processor unit, is coupled to the memory and executes instruction bytecodes obtained from the memory.

The stack machine includes a program counter containing an address of a first instruction bytecode to be decoded.

A program counter calculator is coupled to the program counter and provides the program counter with the address of the first instruction bytecode to be decoded. The program counter calculator includes a match input.

A register contains instruction bytecodes including the first instruction bytecode and a second instruction bytecode following the first instruction.

Decode logic is coupled to the register and to the program counter calculator and decodes the first instruction bytecode from the register.

Pre-decode logic has a match output connected with the match input of the program counter calculator and is coupled to the second instruction bytecode in the register. The pre-decode logic decodes the second instruction bytecode while the decode logic is decoding the first instruction bytecode and selectively provides a match signal to the program counter calculator to increment the program counter past the second instruction bytecode.

In contrast, US 6,014,735 to Chennupaty discloses:

> FIG. 1 illustrates that the processor 110 includes a decode unit 116, a set of registers 114, an execution unit 112, and an internal bus 111 for executing instructions. Of course, the processor 110 contains additional circuitry, which is not necessary to understanding the invention. The decode unit 116, registers 114 and execution unit 112 are coupled together by the internal bus 111. The decode unit 116 is used for decoding instructions received by processor 110 into control signals and/or microcode entry points. In response to these control signals and/or

microcode entry points, the execution unit 112 performs the appropriate operations. The decode unit 116 may be implemented using any number of different mechanisms (e.g., a look-up table, a hardware implementation, a PLA, etc.). column 2, lines 40-54

Instruction Decoding Using Prefixes

FIG. 3 is a diagram illustrating a circuit 300 to decode the instruction. The circuit 300 includes an instruction buffer 310, a prefix and escape detector 320, a decoder enable circuit 330, and an opcode decoder 340. The prefix and escape detector 320, the decoder enable circuit 330, and the opcode decoder 340 form a portion of the decode unit 116 in FIG. 1.

The instruction buffer 310 stores the instructions fetched from the external memory. Typically, the instruction buffer 310 is implemented as an instruction cache. For illustrative purposes, an instruction is assumed to comprise three bytes: The first byte corresponds to I.sub.N to I.sub.N+7, the second byte corresponds to I.sub.K to I.sub.K+7, and the third byte corresponds to I.sub.M to I.sub.M+7, where I.sub.N to I.sub.N+7, I.sub.K to I.sub.K+7, and I.sub.M to I.sub.M+7 refer to the bit positions of the instruction word.

The prefix and escape detector 320 receives the instruction bits I.sub.N to I.sub.N+7, I.sub.K to I.sub.K+7, and detects a set of predefined prefixes and/or escape codes used as part of the new instruction set. The values of these prefixes are selected so that they are the same as those prefixes that are used for the regular instruction set. The decoder enable circuit 330 combines the results of the prefix and escape detector 320 to generate enable or select signals to the individual opcode decoder. The opcode decoder 340 receives the instruction bits I.sub.N to I.sub.N+7, I.sub.K to I.sub.K+7, and I.sub.M to I.sub.M+7 and performs the decoding function for the individual types of instructions. column 5, lines 1-26

The Channupaty patent thus discloses a system with a single processor with serial decoding of instructions to determine prefixes. Apparently there is no stack machine, no pre-decoding of a second bytecode while decoding a first bytecode, and no change of a program counter in response to the pre-decoding.

The patent to Narayan, US 6,161,172, and the publication of Leijten, Pub. No. 202/0,116,598, also apparently fail to disclose any stack machine, any pre-decoding of a second bytecode while decoding a first bytecode, and any change of a program counter in response to the pre-decoding.

New claim 32 distinguishes over the Chennupaty and Narayan patents and Leijten publication with the limitations of a system comprising a memory containing instructions; a main processor unit coupled to the memory and executing instructions obtained from the memory; a stack machine, separate from the main processor unit, coupled to the memory and executing instruction bytecodes obtained from the memory, the stack machine including: a program counter containing an address of a first instruction bytecode to be decoded; a program counter calculator coupled to the program counter and providing the program counter with the address of the first instruction bytecode to be decoded, the program counter calculator including a match input; a register containing instruction bytecodes including the first instruction bytecode and a second instruction bytecode following the first instruction; decode logic coupled to the register and to the program counter calculator and decoding the first instruction bytecode from the register; and pre-decode logic having a match output connected with the match input of the program counter calculator and being coupled to the second instruction bytecode in the register, the pre-decode logic decoding the second instruction bytecode while the decode logic is decoding the first instruction bytecode and selectively providing a match signal to the program counter calculator to increment the program counter past the second instruction bytecode.

Claim 32 stands allowable.

Independent process claim 36 also stands allowable for substantially the same reasons as claim 32.

The application is in allowable form and the claims distinguish over the cited references. Applicants respectfully request reconsideration or further examination of this application.

Respectfully Submitted,

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